REMARKS

Reconsideration of the present application as amended is respectfully requested.

In the Final Office Action, claims 1-9, 21, and 23 were pending. Claims 1-9, 21, and 23 were rejected. A response was filed and an advisory action was issued. In the advisory action, the response was not deemed to be persuasive.

In this response, no claim has been canceled. Claims 1, 3-4, 6, 8-9, 21, and 23 have been amended. New claims 25-36 have been added. Thus, claims 1-9, 21, 23, and 25-36 remain pending. No new matter has been added.

Claims 1-9, 21, and 23 are rejected under 35 U.S.C. §112, first paragraph. The Examiner objected to the limitation of a wait control logic that signals a processor to indicate that the requested data is ready to be read on a next processor cycle if the requested data is in the cache memory. The Examiner stated that the above limitation is not supported in the description.

Accordingly, claims 1 and 6 have been amended to particularly point out and distinctly claim, in full, clear, concise, and exact terms, the subject matter which Applicant regards as his invention. The support of the amended claims 1 and 6 can be found on page 8 of the present application. Withdrawal of the rejections is respectfully requested.

Claims 1-9 are rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,263,398 of Taylor et al. ("Taylor"). Applicant respectfully submits that claims 1-9, 21, and 23 include limitations that are not disclosed by Taylor. In particular, independent claim 1 includes a memory device that includes a wait control logic coupled to a processor, a main memory, and a cache memory, where the wait control logic signals the processor whether the data currently requested is ready to be read, the wait control logic transmitting a first signal having a duration of one clock cycle to the processor when data currently requested is in the cache memory, and the wait control logic transmitting a second signal having a duration of multiple clock cycles when the data currently requested is not in the cache memory. These limitations are absent from Taylor.

In the Office Action, the Examiner stated:

> "AS to claims 1 and 6, Taylor discloses the recited memory device integrated with cache (see Abstract, Figure 1, and column 3 lines 7-35), and stores recently accessed data at 14 and associated addresses at 24. Taylor also additionally teaches the recited wait control signal to the extent disclosed (see 37 CFR 112 rejection above), see signal READY 32 in Fig. 1, and described at col. 5 lines 19-24 and 56-62."

(11/17/2003 Office Action, page 3, emphasis added).

Applicant respectfully disagrees. Figure 1 and its corresponding of Taylor description fail to disclose a wait control logic as claimed in the present application. In order to anticipate claim 1, Taylor has to disclose every limitations as claimed in claim 1. Since there is no wait control logic disclosed by Taylor, Taylor cannot anticipate claim 1.

Even if, for the sake of the argument, the READY signal of Taylor implicated a wait control logic, Taylor still fails to disclose a wait control logic that is coupled to a processor, a main memory, a cache memory. Furthermore, most importantly, Taylor fails to disclose a wait control logic that signals the processor whether the data currently requested is ready to be read, the wait control logic transmitting a first signal having a duration of one clock cycle to the processor when data currently requested is in the cache memory, and the wait control logic transmitting a second signal having a duration of multiple clock cycles when the data currently requested is not in the cache memory. Therefore, independent claim 1 is not anticipated by Taylor.

Independent claim 6 includes limitations similar to those referred by claim 1. Therefore for reasons similar to those discussed above, claim 6 is not anticipated by Taylor.

Given that claims 2-5, 7-9, 21, 23, and 25-36 depend from one of the above independent claims, it is respectfully submitted that claims 2-5, 7-9, 21, 23, and 25-36 are also not anticipated by Taylor. Withdrawal of the rejections is respectfully requested.

With respect to claims 2 and 7, claims 2 and 7 include an address latch logic to receive the addresses of the requested data, an address cache memory coupled to the address latch logic and the wait control logic to store the addresses, and a data cache memory coupled to the address cache memory and the main memory to store the data. Applicant respectfully submits that the above limitations are absent

from Taylor. The Examiner contends that Figure 1 of Taylor reads on the above limitations. Specifically, the Examiner stated:

> "As to claims 2-4 and 7-9, Taylor discloses address latch logic 18, 20, address cache and comparison at 24, and data cache 14. See Fig. 1, and col. 4, lines 56-66, and col. 5, lines 60-62."

(11/17/2003 Office Action, page 3, emphasis added).

Applicant respectfully disagrees. There is no address cache memory shown in Figure 1 of Taylor. The compare block 24 does not include an address cache, particularly, an address cache memory coupled to the address latched logic and the wait control logic to store the addresses of the recently accessed data and to store the address of the requested data after the requested data has been fetched.

Even if, for the sake of the argument, the compare block 24 included an address cache memory, Taylor still fails to disclose an address cache memory that is coupled to the wait control logic to store the addresses of the recently accessed data and to store the address of the requested data after the requested data has been fetched. Taylor still fails to disclose a data cache memory coupled to the address cache memory and the main memory to store the recently accessed data, where the data cache memory receives data from the main memory if the data requested is not in the data cache memory.

With respect to claims 3 and 8, claims 3 and 8 include a comparator coupled to the address latch logic and the address cache memory, where an output of the comparator is coupled to the wait control logic to cause the wait control logic to send a signal to the processor dependent upon whether the address stored in the address latch logic is found in the address cache memory. Applicant respectfully submits that these limitations are also absent from Taylor.

The Examiner contends that compare block 24 of Taylor reads on the above limitations. Applicant respectfully disagrees. There is no showing or suggestion that compare block 24 includes a comparator and an address cache memory in Taylor. Even if, for the sake of the argument, the compare block 24 might include a comparator and an address cache memory, Taylor still fails to disclose or suggest an output of the comparator coupled to the wait control logic to cause the wait control logic to

send a signal to the processor indicating whether the address stored in the address latch logic is found in the address cache memory.

With respect to claims 4 and 9, claims 4 and 9 include limitations that the comparator causes the wait control logic to assert a signal having one cycle to the processor to allow the processor to read in a next cycle the requested data presented by the data cache memory, if the address of the requested data is found in the data cache memory. Applicant respectfully submits that these limitations are also absent from Taylor.

The Examiner contends that Figure 4 of Taylor reads on the above limitations referred by claims 4 and 9. Applicant respectfully disagrees. Figures 4A and 4B of Taylor are flow diagrams illustrating a process or processes. Applicant respectfully submits that Figures 4A and 4B fail to disclose or suggest a comparator causes the wait control logic to assert a signal having one cycle to the processor to allow the processor to read in a next cycle the requested data presented by the data cache memory, if the address of the requested data is found in the data cache memory.

In the advisory action, the Examiner stated that "at minimum, all elements in the device are coupled with one another" (2/10/2004 Advisory Action, page 2). However, in order to anticipate a claim, all limitations of the claim must be taught by Taylor. The structures and configurations are integral parts of a memory design. It is irrelevant whether Taylor teaches one or more elements that are minimally coupled to each other. It is respectfully submitted that the limitations set forth above are not disclosed or suggested by Taylor.

Claims 1-9, 21, and 23 are rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,288,923 of Sakamoto ("Sakamoto") in view of the alleged admitted prior art. Applicant respectfully submits that neither Sakamoto nor the alleged admitted prior art, individually or in combination, discloses or suggests the above discussed limitations. Therefore, at least for the reasons similar to those discussed above, claims 1-9, 21, and 23 are patentable over Sakamoto in view of the alleged admitted prior art. Withdrawal of the rejections is respectfully requested.

In view of the foregoing, Applicant respectfully submits the present application is now in condition for allowance. If the Examiner believes a telephone conference would expedite or assist in the allowance of the present application, the Examiner is invited to call the undersigned attorney at (408) 720-8300.

Please charge Deposit Account No. 02-2666 for any shortage of fees in connection with this response.

Respectfully submitted,
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN

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